

MC74HC244A

Octal 3-State Noninverting Buffer/Line Driver/ Line Receiver

High-Performance Silicon-Gate CMOS

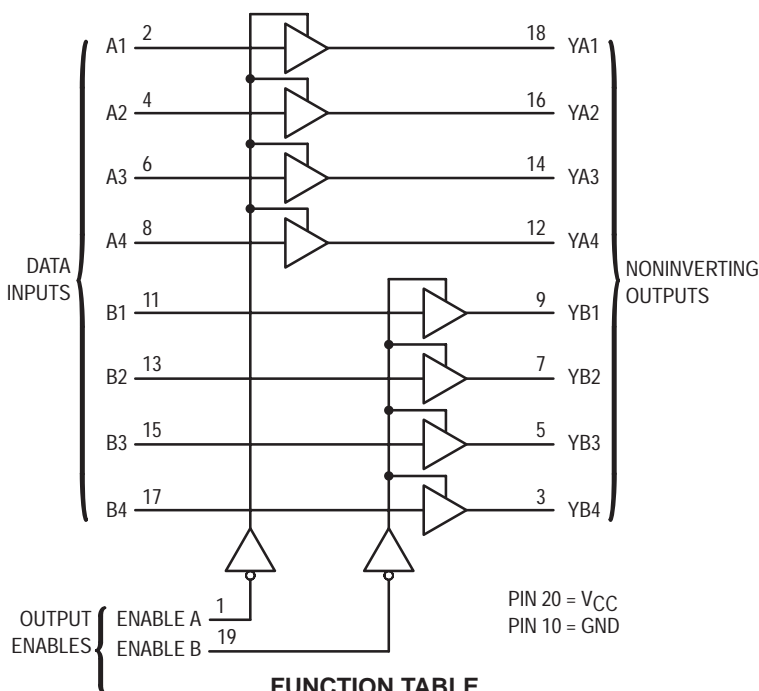
The MC74HC244A is identical in pinout to the LS244. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This octal noninverting buffer/line driver/line receiver is designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has noninverting outputs and two active-low output enables.

The HC244A is similar in function to the HC240A.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 136 FETs or 34 Equivalent Gates

LOGIC DIAGRAM



FUNCTION TABLE

| Inputs | | Outputs |
|--------------------|------|---------|
| Enable A, Enable B | A, B | YA, YB |
| L | L | L |
| L | H | H |
| H | X | Z |

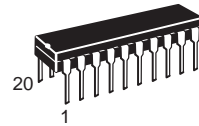
Z = high impedance



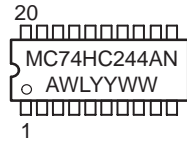
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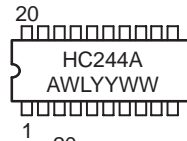
MARKING DIAGRAMS



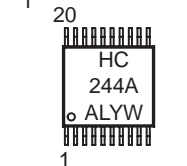
PDIP-20
N SUFFIX
CASE 738



SOIC WIDE-20
DW SUFFIX
CASE 751D

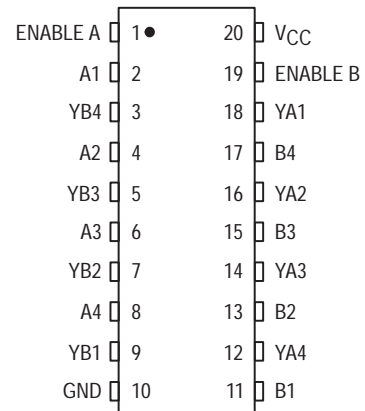


TSSOP-20
DT SUFFIX
CASE 948E



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

| Device | Package | Shipping |
|----------------|-----------|-------------|
| MC74HC244AN | PDIP-20 | 1440 / Box |
| MC74HC244ADW | SOIC-WIDE | 38 / Rail |
| MC74HC244ADWR2 | SOIC-WIDE | 1000 / Reel |
| MC74HC244ADT | TSSOP-20 | 75 / Rail |
| MC74HC244ADTR2 | TSSOP-20 | 2500 / Reel |

MC74HC244A

MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|------------------|---|--------------------------------|------|
| V _{CC} | DC Supply Voltage (Referenced to GND) | - 0.5 to + 7.0 | V |
| V _{in} | DC Input Voltage (Referenced to GND) | - 0.5 to V _{CC} + 0.5 | V |
| V _{out} | DC Output Voltage (Referenced to GND) | - 0.5 to V _{CC} + 0.5 | V |
| I _{in} | DC Input Current, per Pin | ± 20 | mA |
| I _{out} | DC Output Current, per Pin | ± 35 | mA |
| I _{CC} | DC Supply Current, V _{CC} and GND Pins | ± 75 | mA |
| PD | Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package† | 750 500 450 | mW |
| T _{stg} | Storage Temperature | - 65 to + 150 | °C |
| T _L | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC, SSOP or TSSOP Package) | 260 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: - 7 mW/°C from 65° to 125°C
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit | |
|------------------------------------|--|---|-----------------|--------------------|----|
| V _{CC} | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V | |
| V _{in} , V _{out} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V _{CC} | V | |
| T _A | Operating Temperature, All Package Types | - 55 | + 125 | °C | |
| t _r , t _f | Input Rise and Fall Time (Figure 1) | V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V | 0 0 0 | 1000 500 400 | ns |

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limit | | | Unit |
|-----------------|-----------------------------------|---|---|------------------|--------|---------|------|
| | | | | - 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{out} = V _{CC} - 0.1 V I _{out} ≤ 20 μA | 2.0 | 1.5 | 1.5 | 1.5 | V |
| | | | 3.0 | 2.1 | 2.1 | 2.1 | |
| | | | 4.5 | 3.15 | 3.15 | 3.15 | |
| | | | 6.0 | 4.2 | 4.2 | 4.2 | |
| V _{IL} | Maximum Low-Level Input Voltage | V _{out} = 0.1 V I _{out} ≤ 20 μA | 2.0 | 0.5 | 0.5 | 0.5 | V |
| | | | 3.0 | 0.9 | 0.9 | 0.9 | |
| | | | 4.5 | 1.35 | 1.35 | 1.35 | |
| | | | 6.0 | 1.8 | 1.8 | 1.8 | |
| V _{OH} | Minimum High-Level Output Voltage | V _{in} = V _{IH} I _{out} ≤ 20 μA | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | | 6.0 | 5.9 | 5.9 | 5.9 | |
| | | | V _{in} = V _{IH} I _{out} ≤ 2.4 mA I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA | 3.0 | 2.48 | 2.34 | |
| 4.5 | 3.98 | 3.84 | 3.7 | | | | |
| 6.0 | 5.48 | 5.34 | 5.2 | | | | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{in} = V _{IL} I _{out} ≤ 20 μA | 2.0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5 | 0.1 | 0.1 | 0.1 | |
| | | | 6.0 | 0.1 | 0.1 | 0.1 | |
| | | | V _{in} = V _{IL} I _{out} ≤ 2.4 mA I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA | 3.0 | 0.26 | 0.33 | |
| 4.5 | 0.26 | 0.33 | 0.4 | | | | |
| 6.0 | 0.26 | 0.33 | 0.4 | | | | |

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limit | | | Unit |
|-----------------|--|---|----------------------|------------------|--------|---------|------|
| | | | | - 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| I _{in} | Maximum Input Leakage Current | V _{in} = V _{CC} or GND | 6.0 | ± 0.1 | ± 1.0 | ± 1.0 | μA |
| I _{OZ} | Maximum Three-State Leakage Current | Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND | 6.0 | ± 0.5 | ± 5.0 | ± 10 | μA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{in} = V _{CC} or GND I _{out} = 0 μA | 6.0 | 4.0 | 40 | 160 | μA |

NOTE: Information on typical parametric values and high frequency or heavy load considerations can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|--|---|--------------------------|-----------------------|-----------------------|-----------------------|------|
| | | | - 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3) | 2.0 3.0 4.5 6.0 | 96 50 18 15 | 115 60 23 20 | 135 70 27 23 | ns |
| t _{PLZ} , t _{PHZ} | Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4) | 2.0 3.0 4.5 6.0 | 110 60 22 19 | 140 70 28 24 | 165 80 33 28 | ns |
| t _{PZL} , t _{PZH} | Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4) | 2.0 3.0 4.5 6.0 | 110 60 22 19 | 140 70 28 24 | 165 80 33 28 | ns |
| t _{TLH} , t _{THL} | Maximum Output Transition Time, Any Output (Figures 1 and 3) | 2.0 3.0 4.5 6.0 | 60 23 12 10 | 75 27 15 13 | 90 32 18 15 | ns |
| C _{in} | Maximum Input Capacitance | — | 10 | 10 | 10 | pF |
| C _{out} | Maximum Three-State Output Capacitance (Output in High-Impedance State) | — | 15 | 15 | 15 | pF |

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

| C _{PD} | Power Dissipation Capacitance (Per Buffer)* | Typical @ 25°C, V _{CC} = 5.0 V | |
|-----------------|---|---|--|
| | | 34 | |
| | | pF | |

* Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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SWITCHING WAVEFORMS

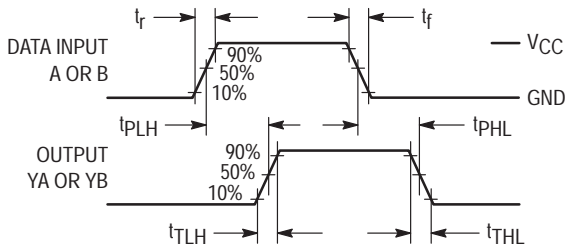


Figure 1.

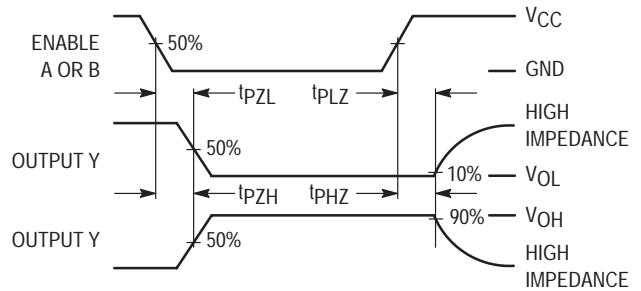
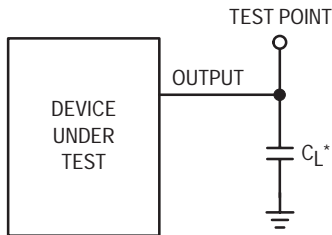


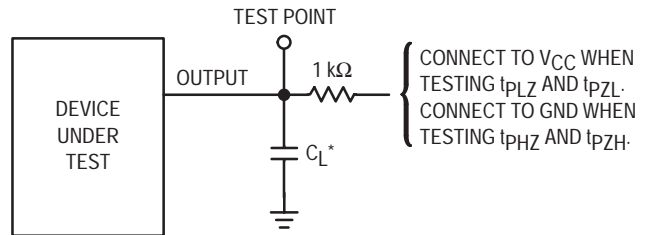
Figure 2.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 3. Test Circuit



*Includes all probe and jig capacitance

Figure 4. Test Circuit

PIN DESCRIPTIONS

INPUTS

A1, A2, A3, A4, B1, B2, B3, B4
(Pins 2, 4, 6, 8, 11, 13, 15, 17)

Data input pins. Data on these pins appear in noninverted form on the corresponding Y outputs, when the outputs are enabled.

CONTROLS

Enable A, Enable B (Pins 1, 19)

Output enables (active-low). When a low level is applied to these pins, the outputs are enabled and the devices

function as noninverting buffers. When a high level is applied, the outputs assume the high impedance state.

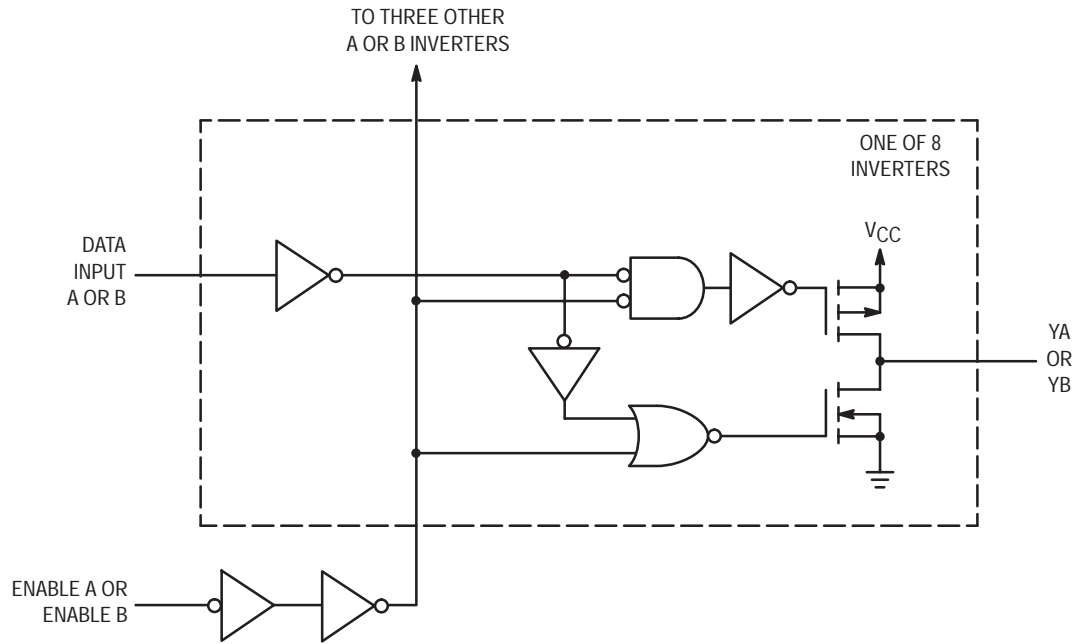
OUTPUTS

YA1, YA2, YA3, YA4, YB1, YB2, YB3, YB4
(Pins 18, 16, 14, 12, 9, 7, 5, 3)

Device outputs. Depending upon the state of the output-enable pins, these outputs are either noninverting outputs or high-impedance outputs.

MC74HC244A

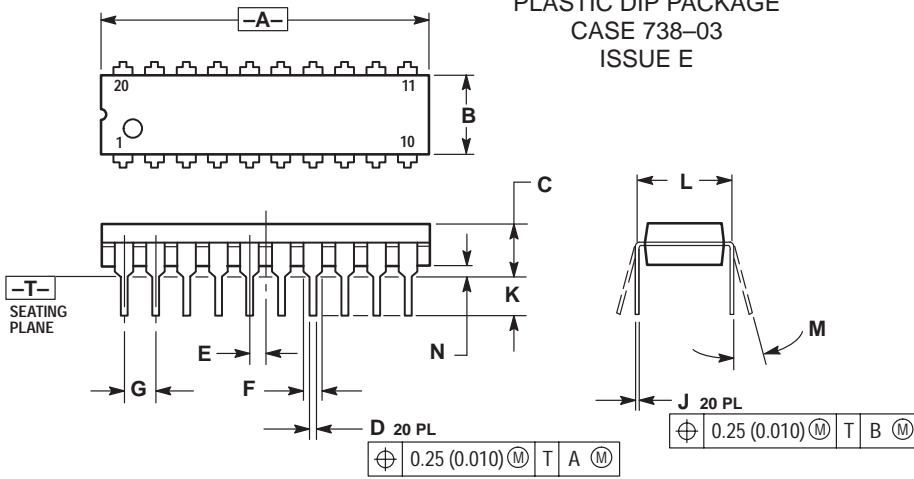
LOGIC DETAIL



MC74HC244A

PACKAGE DIMENSIONS

PDIP-20
N SUFFIX
PLASTIC DIP PACKAGE
CASE 738-03
ISSUE E

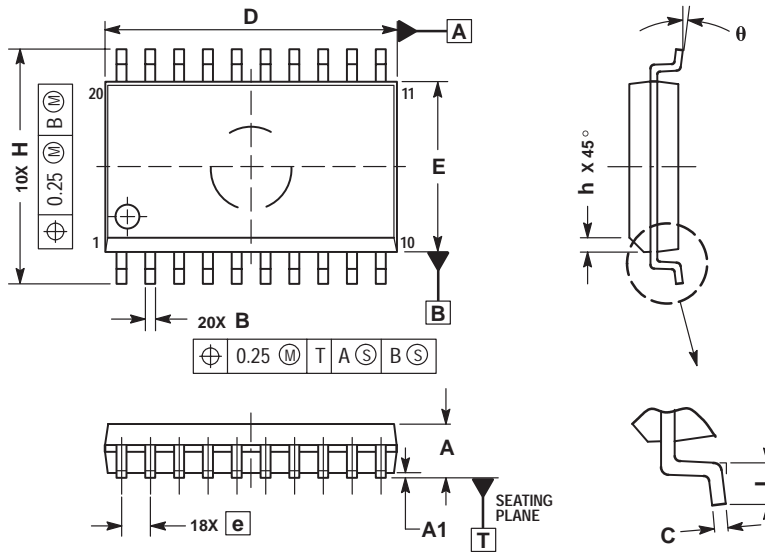


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.010 | 1.070 | 25.66 | 27.17 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.150 | 0.180 | 3.81 | 4.57 |
| D | 0.015 | 0.022 | 0.39 | 0.55 |
| E | 0.050 BSC | | 1.27 BSC | |
| F | 0.050 | | 1.27 | |
| G | 0.100 BSC | | | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.140 | 2.80 | 3.55 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.020 | 0.040 | 0.51 | 1.01 |

SO-20
DW SUFFIX
CASE 751D-05
ISSUE F



NOTES:

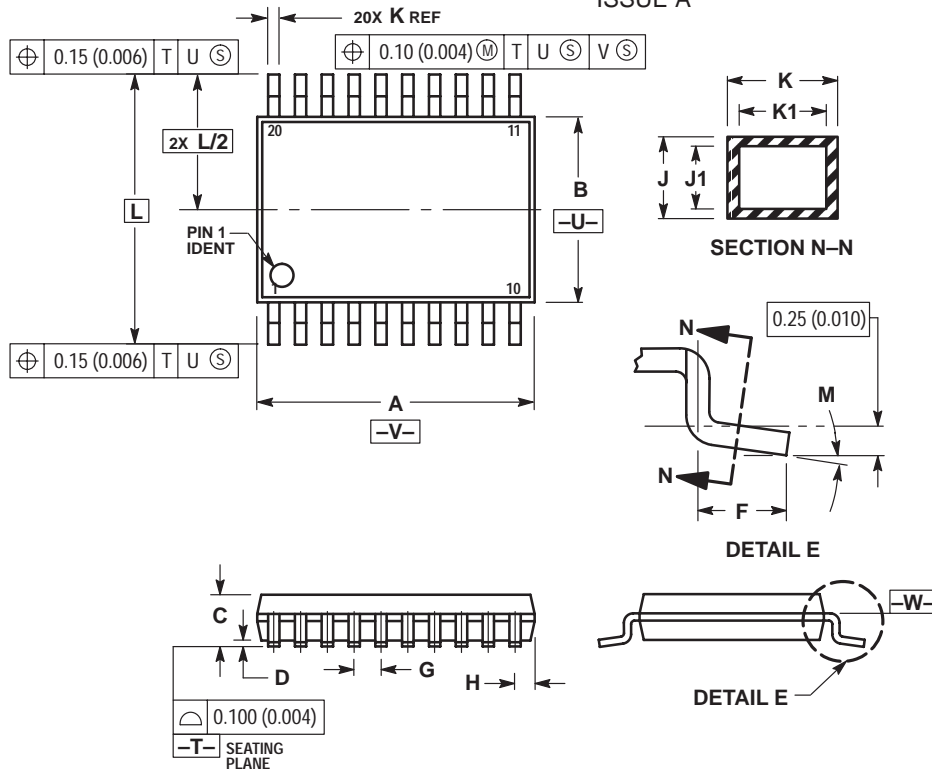
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

MC74HC244A

PACKAGE DIMENSIONS


TSSOP-20
DT SUFFIX
CASE 948E-02
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

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